REMARKS

The specification has been revised to correct various self-evident errors in grammar, typing, punctuation, singular-versus-plural case, and figure identification. On page 5, the second paragraph of the Summary-of-the-Invention section has been revised to conform more closely to the claims in that the five core semiconductor regions of the present electrostatic discharge ("ESD") device can have an n-p-n-p-n or p-n-p-n-p arrangement. On page 13, coordinate positions "(I_t, V_t)" and "(I_h, V_h)" have been respectively changed to "(V_t, I_t)" and "(V_h, I_h)" to conform the specification to the coordinate-position convention employed in Fig. 6. Two parenthetical sentences have been added to page 18 to identify a pair of electrical connections that are needed to enable Fig. 12 to conform with Fig. 13 and with the text dealing with Figs. 12 and 13.

The specification has also been revised in several instances to eliminate usage of the same reference symbol for materially different items. In particular, reference symbol "30", as utilized on page 3 in reference to the curved arrows shown in Fig. 1D, has been changed to "40" since reference symbol "30" is used earlier for an npn transistor. Reference symbols "126" and "130" as employed on page 15 respectively for a section of n-well 116 and the curved arrows shown in Fig. 7 have been respectively changed to "146" and "148" since reference symbols "126" and "130" are respectively used earlier for a p-n junction and an npn transistor.

Reference symbols "130" and "132" as employed on page 16 for the curved arrows shown in Fig. 8A have been respectively changed to "152" and "154" since reference symbols "130" and "132" are respectively used earlier for an npn transistor and a resistor. Reference symbols "130" and "132" as employed on page 16 for the curved arrows shown in Fig. 10A have been respectively changed to "172" and "174" for the same reason. Reference symbols "130", "132", "134", and "136" as employed on page 16 for the curved arrows shown in Fig. 9A have been respectively changed to "162", "164", "166", and "168" since reference symbols "130", "132", "134", and "136" are respectively used earlier for an npn transistor and three resistors.

Reference symbol "130" as utilized on page 16 for the curved arrows shown in Fig. 11A has been changed to "178" since reference symbol "130" is, as indicated above,

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

utilized earlier for an npn transistor. Taking note of the fact that the arrows represented by reference symbol "130" in Fig. 11A variously correspond to the arrows represented by reference symbols "130", "132", "134", and "136" in Figs. 8A, 9A, and 10A, a sentence has been added to page 16 to indicate that, using the revised labeling presented herein, arrows "178" variously correspond to arrows "152", "154", "162", "164", "166", "168", "172", and "174" in Figs. 8A, 9A, and 10A. By the accompanying amendment to the drawings, Applicants' Attorney has requested that the drawings be amended to conform to the preceding reference-symbol changes to the specification.

The title and abstract have been revised to conform more closely to the pending claims.

Turning to the claims, dependent Claim 42 has been amended to identify the number of the claim from which Claim 42 depends. No claims have been added or canceled. Accordingly, Claims 2, 3, 5 - 8, 21, 22, and 26 - 42 are still pending.

Taking note of the fact that Claims 33 - 42 are method claims while the remainder of the claims pending at the time of Office Action are device claims, the Examiner has withdrawn Claims 33 - 42 from consideration as being constructively directed to a non-elected invention. The Examiner particularly states that:

> Newly submitted claims 33-42 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: the invention originally claimed (in the active claims in the previously office action) is directed to a device, while the invention claimed in claims 33-42 is directed to a method.
>
> Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 33-42 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

The withdrawal of Claims 33 - 42 from consideration in the present application is respectfully traversed.

Applicants' Attorney believes that the Examiner has acted in haste in withdrawing Claims 33 - 42 from consideration. Claims 33 - 42 are indeed method claims while the remainder of the claims pending at the time of the Office Action, and still pending, are device claims. However, Claims 33 - 42 are not fabrication claims. Instead, Claims 33 - 42 are

directed to a method of using (or operating) an ESD protection device. The remainder of the pending claims, i.e., Nos. 2, 3, 5 - 8, 21, 22, and 26 - 32, are device claims directed to the structure of an ESD protection device.

With respect to issuing a restriction requirement between one or more claims directed to a product (or device) and one or more claims directed to a process (or method) of using the product (or device) section 806.05(h) of the Manual of Patent Examining Procedure ("MPEP") states that:

> A product and a process of using the product can be shown to be distinct inventions if either or both of the following can be shown: (A) the process of using as claimed can be practiced with another materially different product; or (B) the product as claimed can be used in a materially different process.
>
> The burden is on the examiner to provide an example, but the example need not be documented.
>
> If the applicant either proves or provides a convincing argument that the alternative use suggested by the examiner cannot be accomplished, the burden is on the examiner to support a viable alternative use or withdraw the requirement.

During the prosecution of a U.S. utility patent application, the distinctiveness requirement of MPEP section 806.05(h) must be met at any time that a U.S. patent examiner issues a restriction requirement between a product claim and a claim directed to a method of using the product. MPEP section 821.03, cited by the present Examiner, repeats 37 CFR 1.145 in stating that:

> Claims added by amendment following action by the examiner, MPEP § 818.01, § 818.02(a), to an invention other than previously claimed, should be treated as indicated by 37 CFR 1.145.
>
> *37 CFR 1.145. Subsequent presentation of claims for different invention.*
>
> If, after an office action on an application, the applicant presents claims directed to an invention distinct from and independent of the invention previously claimed, the applicant will be required to restrict the claims to the invention previously claimed if the amendment is entered, subject to reconsideration and review as provided in §§ 1.143 and 1.144.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

The Examiner has not met the distinctiveness requirement imposed by MPEP section 806.05(h) and 37 CFR 1.145 as prescribed in MPEP section 821.03 so as to justify withdrawing Claims 33 - 42 from consideration in this application.

More particularly, dependent Claim 38 is specifically directed to a method of using the ESD protection device of independent Claim 8. Dependent Claim 40 is similarly directed to a method of using the ESD protection device of independent Claim 21. Accordingly, Claims 38 and 40 along with their dependent Claims 39, 41, and 42 are to be examined in this application.

Furthermore, Claims 38 and 40 both depend from independent Claim 33. Hence, Claim 33 is also to be examined in this application. The same applies to Claims 34 - 37 since they depend (directly or indirectly) from Claim 33. The net result is that all of Claims 33 - 42 are to be considered, and thus examined, in the present application.

Claims 2, 3, 5 - 8, 21, 22, and 26 - 32 have been rejected under 35 USC 112 for failing to comply with the written description requirement as containing subject matter "not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention". This rejection is respectfully traversed.

The Examiner alleges that:

> Claims 8 and 21 each recite the combination of the subject matters that the first terminal is connected to the first and second semiconductor regions and that the first resistor is coupled between the first terminal and the second semiconductor region, which is not fully supported by the original disclosure. According to the relevant embodiments shown in Figs. 13 and 14, only the first resistor (758) is coupled to the second semiconductor region, while the first terminal (A) is not directly coupled to the second semiconductor region therein. It is further noted that, in the embodiment of Fig. 12, only the first terminal (A) is coupled to the second semiconductor region (128 [sic, 114] through the P+ region), while the first resistor (758) is not directly coupled to the second semiconductor region therein.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

The Examiner appears to have missed the fact that the semiconductor region which, in the specification, implements the second semiconductor region of each of independent Claims 8 and 21 includes a heavily doped portion which directly contacts the terminal that implements the first terminal of each of Claims 8 and 21. Also, the semiconductor region

which, in the specification, implements the fourth semiconductor region of each of Claims 8 and 21 similarly includes a heavily doped portion which directly contacts the terminal that implements the second terminal of each of Claims 8 and 21. For instance, assume that p-type semiconductor regions 114 and 118 respectively correspond to the second and fourth semiconductor regions of each of Claims 8 and 21.

Subject to providing Fig. 12 with the missing reference symbols "112", "114", and "122" for the regions respectively labeled "112", "114", and "122" in Fig. 3, first terminal A is directly connected to p-type region 122 and n-type first semiconductor region 112 as shown in Figs. 3 and 12. Region 122 is a heavily doped contact portion of p-type second semiconductor region 114. Accordingly, first terminal A is directly connected to both first semiconductor region 112 and second semiconductor region 114 so as to support the limitation of each of Claims 8 and 21 that the first terminal is connected to both the first and second semiconductor regions.

Additionally, second terminal K is directly connected to p-type region 124 and n-type fifth semiconductor region 120. Region 124 is a heavily doped contact portion of p-type fourth semiconductor region 118. Hence, second terminal K is directly connected to both fifth semiconductor region 120 and fourth semiconductor region 118 so as to support the limitation of each of Claims 8 and 21 that the first terminal is connected to both the fourth and fifth semiconductor regions. The specification thereby supports both the limitation that the first terminal is connected to the first and second semiconductor regions and the limitation that the second terminal is connected to the fourth and fifth semiconductor regions.

In regard to the Examiner's comment "that, in the embodiment of Fig. 12, only the first terminal (A) is coupled to the second semiconductor region (128 [sic, 114] through the P+ region), while the first resistor (758) is not directly coupled to the second semiconductor region therein", the specification has been revised to provide that a line, not shown in Fig. 12, connects the base of npn transistor 130 to a node (on the line) between resistor 758 and current source 772. The specification has also been revised to provide that a line, likewise not shown in Fig. 12, connects the base of npn transistor 150 to a node (on the line) between resistor 756 and current source 770.

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

The preceding two lines are shown in Fig. 13. Even though these two lines are not depicted in Fig. 12, the foregoing revisions to the specification bring the content of Fig. 12 into conformity with Fig. 13.

Second semiconductor region 114 serves as the base of transistor 130. Consequently, the line (shown in Fig. 13 but not in Fig. 12) by which the base of transistor 130 is connected to the node between resistor 758 and current source 772 connects first resistor 758 to second semiconductor region 114. Since first resistor 758 is connected to first terminal A, the specification supports the limitation of each of Claims 8 and 21 that the first resistor is coupled between the first terminal and the second semiconductor region.

Fourth semiconductor region 118 serves as the base of transistor 150. Hence, the line (likewise shown in Fig. 13 but not in Fig. 12) by which the base of transistor 150 is connected to the node between resistor 756 and current source 770 connects second resistor 756 to fourth semiconductor region 118. With second resistor 756 being connected to second terminal K, the specification supports the limitation of each of Claims 8 and 21 that the second resistor is coupled between the second terminal and the fourth semiconductor region.

The preceding comments show that the specification, including Figs. 12 and 13, supports all the claim limitations that the Examiner has alleged as not having specification support. The 35 USC 112 lack-of-support rejection of Claims 2, 3, 5 - 8, 21, 22, and 26 - 32 should therefore be withdrawn.

Claims 2, 3, 5 - 8, 21, 22, and 26 - 32 have been rejected under 35 USC 112 for failure to satisfy the enablement requirement as containing subject matter "not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention". This rejection is respectfully traversed.

The Examiner alleges that:

> Claims 8 and 21 each recite the combination of the subject matters that the first terminal is connected to the first and second semiconductor regions and that the first resistor is coupled between the first terminal and the second semiconductor region. However, if the first terminal is connected to both of the first and second semiconductor regions, as defined in these claims, the first terminal and the second semiconductor region are then effectively shortened [sic, shorted] together. It then would effectively shorten [sic, short] the two ends of the first resistor if the first resistor is truly coupled between the first

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

terminal and the second semiconductor region. Similarly, the recited second resistor would also be shortened [sic, shorted]. It is not clear how the recited first and second resistors could be functional if each of the two resistors has already been shortened [sic, shorted].

The Examiner here appears to have overlooked the fact that semiconductor material has inherent resistance commonly referred to as parasitic resistance. Current flowing through a semiconductor region encounters its parasitic resistance. In modeling a semiconductor device as group of a ideal resistors, capacitors, inductors, electrical conductors, and the like, an element representing the parasitic resistance of a semiconductor region is commonly shown in a model of the semiconductor device. However, parasitic resistance is simply an inherent property of a semiconductor region and is not electrically separate from the semiconductor region. The recitation in independent Claims 8 and 21 that the first terminal is "connected" to both the first and second semiconductor regions thus inherently includes the fact that each of the two semiconductor regions has some parasitic resistance.

Referring to Figs. 12 and 13 for the situation in which the first and second semiconductor regions of each of Claims 8 and 21 are implemented with n-type first semiconductor region 112 and p-type second semiconductor region 114, including heavily doped p-type contact portion 122, item 132 is the parasitic resistance of second semiconductor region 114 along the current path from contact portion 122 to n-type third semiconductor region 116. Although the recitations in each of Claims 8 and 21 (a) that the first terminal is "connected" to the first and second semiconductor regions and (b) that the first region is "coupled" between the first terminal and the second semiconductor region means that the two ends of the first resistor are coupled together, these two recitations do not mean that the two ends of the resistor are electrically shorted to each other.

Instead, the two ends of the first resistor in each of Claims 8 and 21 are coupled together through the second semiconductor region's parasitic resistance implemented with resistor 132 in the specification. When current flows through the first and second semiconductor regions, the two ends of the resistor are at different electrical potentials depending on the magnitude of the current and the value of the parasitic resistance of the second semiconductor region. Due to the parasitic resistances of the first and second semiconductor regions, specifically the second semiconductor region's parasitic resistance, the recitations in each of Claims 8 and 21 (a) that the first terminal is "connected" to the first

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779

and second semiconductor regions and (b) that the first resistor is coupled between the first terminal and the second semiconductor region are enabled by the specification so that the first resistor performs an actual function.

Similar comments apply to the recitations in each of Claims 8 and 21 (a) that the second terminal is "connected" to the fourth and fifth semiconductor regions and (b) that the second resistor is "coupled" between the second terminal and the fourth semiconductor region. Although these two recitations mean that the two ends of the second resistor are coupled together, the two recitations do not mean that the two ends of the second resistor are electrically shorted to each other.

Instead, the two ends of the second resistor are coupled together through the fourth semiconductor region's parasitic resistance implemented with resistor 138 in the specification. This enables the two ends of the second resistor to be at different electrical potentials when current flows through the fourth and fifth semiconductor regions. The recitations (a) that the second terminal is connected to the fourth and fifth semiconductor regions and (b) that the second resistor is coupled between the second terminal and the fourth semiconductor region are thus enabled by the specification such that the second resistor performs an actual function. For these reasons, the non-enablement rejection Claims of 2, 3, 5 - 8, 21, 22, and 26 - 32 should be withdrawn.

In summary, all of Claims 2, 3, 5 - 8, 21, 22, and 26 - 42 should be considered, and thus examined, in the present application. The 35 USC 112 lack-of-support and non-enablement rejections should be withdrawn. Subject to examining Claims 33 - 42, Claims 2, 3, 5 - 8, 21, 22, and 26 - 42 should be allowed so that the application may proceed to issue.

Please telephone Attorney for Applicant(s) at 650-964-9767 if there are any questions.

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Respectfully submitted,

Ronald J. Meetin

Ronald J. Meetin
Attorney for Applicant(s)
Reg. No. 29,089

210 Central Avenue
Mountain View, CA 94043-4869

Ronald J. Meetin
Attorney at Law
210 Central Avenue
Mountain View, CA
94043-4869
Tel.: 650-964-9767
Fax: 650-964-9779